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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,242	01/25/2001	Melissa D. Cooper	95-360	3543
20736	7590	05/18/2004		
MANELLI DENISON & SELTER 2000 M STREET NW SUITE 700 WASHINGTON, DC 20036-3307				
			EXAMINER TON, ANTHONY T	
			ART UNIT 2661	PAPER NUMBER 4
DATE MAILED: 05/18/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/768,242

**Applicant(s)**

COOPER, MELISSA D.

**Examiner**

Anthony T Ton

**Art Unit**

2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE \_\_\_\_\_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 January 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>3</u> . | 6) <input type="checkbox"/> Other: _____  |

***Claim Objections***

1. **Claim 7** is objected to because of the following informalities:

**In the Claim:** Term “frame output by” in line 3 is not proper since the term “**output**” is not correct in grammar.

Examiner suggests changing this term to “frame **outputted** by”.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1, 6, 7 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tateishi** (US Patent No. 5,383,177) in view of **Payne et al** (US Patent No. 6,347,395).

a) **In Regarding to Claim 1:** **Tateishi** disclosed a method for testing a network switch chip having an expansion port configured for transferring data according to a prescribed protocol (*see Fig.1*), the method comprising:

receiving by an external logic unit an expansion port frame from the expansion port via an expansion bus (*see Fig.1: block 6 (external logic unit), blocks 2a and 3a (expansion port), link IW1-IWn and OWi-OWn (expansion bus); see col.2 lines 26-31: the transmitting section transmits packet data to the under-test-device (hence receiving by the external logic unit); and see Fig.6(b) for expansion port frame*);

generating by the external logic unit a new expansion port frame based on reception of the expansion port frame (*see Fig.8: step 304, communications processing; and see Fig.6(c) for new expansion port frame; in which, the difference in a header h1 "N2 and W2" in comparison to the header h1 "N1 and W1" of the previous frame as shown in Fig.6(b)); and*

outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the network switch chip (*see Fig.8: step 305 store packet data from one output highway; and see Fig.1: block 3a, receiving section*)

**Tateishi failed to explicitly disclose** a network switching chip configured for transferring data. **However, Tateishi clearly disclosed** a packet switching testing apparatus and a under test device as shown in block 1a and block 6 in Fig.1, respectively.

**Payne disclosed** such a network switching chip (*see Fig.3-2: block 310 (network switching chip)*)

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such a chip throughout the under test device of Tateishi, as taught by Payne in order to provide the integrity of segmentation operations, **the motivation being** to reduce space in packaging of electronic devices.

**b) In Regarding to Claim 7: Tateishi disclosed** a test system for testing a network switch chip having an expansion port configured for transferring data according to a prescribed protocol (*see Fig.1*), the system comprising:

an expansion port bus configured for propagation of the expansion port frame outputted by the expansion (*see Fig.1: Link Highways IW1-IWn and OWi-Own*); and

an external logic unit configured for generating a new expansion port frame based on reception of the expansion port frame (*see Fig.1: block 6 (external logic unit); and see Fig.6(b) for expansion port frame*), and outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the network switch chip (*see Fig.8: step 305 store packet data from one output highway; and see Fig.1: block 3a, receiving section*).

**Tateishi failed to explicitly disclose** a network switching chip configured for transferring data. **However, Tateishi clearly disclosed** a packet switching testing apparatus and a under test device as shown in block 1a and block 6 in Fig.1, respectively.

**Payne disclosed** such a network switching chip (*see Fig.3-2: block 310 (network switching chip)*)

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such a chip throughout the under test device of Tateishi, as taught by Payne in order to provide the integrity of segmentation operations, **the motivation being** to reduce space in packaging of electronic devices.

**c) In Regarding to Claim 11: Tateishi disclosed** all aspects of this claim as set forth in claim 7.

**Tateishi failed to explicitly disclose** wherein the external logic unit is implemented using a field programmable gate array.

**Payne disclosed** such wherein the external logic unit is implemented using a field programmable gate array (*see Fig.3-1: block 232 FPGA*)

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such a field programmable gate array throughout the device 6

as shown in Fig.1 of Tateishi, as taught by Payne in order to integrate variety of electronic devices into a user-configurable logic device, **the motivation being** to the complexity of electronic devices and save more space in packaging.

d) **In Regarding to Claim 6:** This claim is rejected for the same reasons as Claim 11 because the apparatus in Claim 11 can be used to practice the method steps of Claim 6.

4. **Claims 2-5 and 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tateishi** (US Patent No. **5,383,177**) in view of **Payne et al** (US Patent No. **6,347,395**) as applied to claims 1 and 7 above, and further in view of **Fowler et al** (US Patent No. **5,721,728**)

a) **In Regarding to Claim 8:** **Tateishi disclosed** all aspects of the claim 8 as set forth in Claim 7.

**Tateishi failed to explicitly disclose** wherein the external logic unit is configured for generating the new expansion port frame by changing data within the received expansion port frame.

**Fowler et al disclosed** such a changing data within the received expansion port frame (*see col.5 lines 53-59: The application layer 14c the generates a second user portion based on the test parameters*).

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such a changing data within the received expansion port frame throughout the packet data frame as shown in Fig.6(c) of Tateishi, as taught by Fowler et al so that such frames can be used in different purposes, **the motivation being** to generate a desire packet frame more faster.

**b) In Regarding to Claim 9: Tateishi, Payne et al. and Fowler et al. disclosed all aspects of this claim as set forth in claims 7 and 8.**

**Tateishi failed to explicitly disclose** wherein the external logic unit is configured for changing data by parsing a header of the expansion port frame to retrieve a source address value from a source address field and a destination address value from a destination address field, the external logic unit inserting the source address value into the destination address field, and the destination address value into the source address field, of the new expansion port frame.

**However, Fowler disclosed** a called party field and a calling party field corresponding to a called party address and calling party address, respectively. When generating a new data (ph-ph packet), application processor uses the corresponding data in the ph-ph packet to generate the called party field and the calling party field as illustrated in Fig.2; wherein the called party field is set equal to the called party address block of test parameters as shown in Fig.3, and the calling party field is set equal to the original called party information passed within the ph-ph packet (*see col.10 lines 10-24*). **Therefore**, it would be obvious that Fowler disclosed such the claimed subject matters of the instant claim.

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such claimed subject matters of the instant claims to the packet, as taught by Fowler so that a desired packet can be generated without creating a new data for the packet header of the packet, **the motivation being** to provision time efficiency and avoid error when creating a new data.

**c) In Regarding to Claim 10: Tateishi, Payne et al. and Fowler et al. disclosed all aspects of this claim as set forth in claims 7-9.**

**Tateishi failed to explicitly disclose** wherein the external logic unit is configured for inserting a new device identifier value into a device identifier field in the new expansion port frame.

**Fowler et al. disclosed** such inserting a new device identifier value into a device identifier field in the new expansion port frame (*see col.4 lines 61-63: PH Number Byte 53 contains a value that identifies the second protocol handler 14*).

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such inserting a new device identifier value into a device identifier field in the new expansion port frame throughout the header of the output data frame as shown in Fig.6(c) of Tateishi, as taught by Fowler so that a desired packet header can be generated without creating a new data for the packet header, **the motivation being** to provision time efficiency and avoid error when creating a new data.

**d) In Regarding to Claims 2-4:** These claims are rejected for the same reasons as Claims 8-10, respectively because the apparatus in Claims 8-10 can be used to practice the method steps of Claims 2-4, respectively.

**e) In Regarding to Claim 5: Tateishi, Payne et al. and Fowler et al. disclosed** all aspects of this claim as set forth in claims 1-4.

**Tateishi failed to explicitly disclose** wherein the external logic unit is implemented using a field programmable gate array.

**Payne disclosed** such wherein the external logic unit is implemented using a field programmable gate array (*see Fig.3-1: block 232 FPGA*)

**It would have been obvious** to one having ordinary skill in the art at the time the invention was made to implement such a field programmable gate array throughout the device 6 as shown in Fig.1 of Tateishi, as taught by Payne in order to integrate variety of electronic devices into a user-configurable logic device, **the motivation being** to the complexity of electronic devices and save more space in packaging.


***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Ton whose telephone number is 703-305-8956. The examiner can normally be reached on M-F: 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W Olms can be reached on 703-305-4703. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ATT  
5/11/2004

  
**KENNETH VANDERPUYE**  
**PRIMARY EXAMINER**

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

## EXAMINER'S CASE ACTION WORKSHEET

Application No. 09/768,242		Legal Instrument Examiner
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CHECK TYPE OF ACTION

DATE OF COUNT

<input checked="" type="checkbox"/> Non-Final Rejection	<input type="checkbox"/> Restriction/Election Only	<input type="checkbox"/> Final Rejection
<input type="checkbox"/> Ex Parte Quayle	<input type="checkbox"/> Allowance	<input type="checkbox"/> Advisory Action
<input type="checkbox"/> Examiner's Answer	<input type="checkbox"/> Reply Brief Noted	<input type="checkbox"/> Non-Entry of Reply Brief
<input type="checkbox"/> Defective Notice of Appeal	<input type="checkbox"/> Interference Disposal SPE _____ (Approval for Disposal)	<input type="checkbox"/> Suspension (Examiner-Initiated) SPE _____ (initial)
<input type="checkbox"/> Defective Appeal Brief	<input type="checkbox"/> SIR Disposal (use only after FAOM)	<input type="checkbox"/> Supplemental Examiner's Amendment
<input type="checkbox"/> Miscellaneous Office Letter (With Shortened Statutory Period Set)	<input type="checkbox"/> Notice of Non-Responsive Amendment (With One Month Time Period set)	<input type="checkbox"/> Miscellaneous Office Letter (No Response Period Set)
<input type="checkbox"/> Abandonment after BPAI Decision	<input type="checkbox"/> Supplemental Action (excluding Examiner's Answer)	<input type="checkbox"/> Response to Rule 312 Amendment
<input type="checkbox"/> Letter Restarting Period for Response (e.g., Missing References)	<input type="checkbox"/> Interview Summary	<input type="checkbox"/> Authorization to Change Previous Office Action SPE: _____ (Initial)
<input type="checkbox"/> Abandonment	<input type="checkbox"/> Express Abandonment Date: _____	<input type="checkbox"/> Other Specify: _____

Examiner's Name: Anthony T Ton

AU: 2661